

US-PAT-NO: 5698869

DOCUMENT-IDENTIFIER: US 5698869 A

TITLE: Insulated-gate transistor having  
narrow-bandgap-source

----- KWIC -----

Brief Summary Text - BSTX (17):

In the meanwhile, if composition (1-x) of Ge of the Si.sub.x Ge.sub.1-x mixed crystal is increased by higher implantation dose of Ge ions etc., misfit dislocations in Si crystal are generated due to the lattice mismatch, which means that the existence of Ge generates distortion in the Si crystal, since the lattice constant or the impurity atom radius of Ge is large by about 4% in comparison with that of Si. Because of this distortion, crystal defects are generated in the direction traversing the pn junction interface between the source and drain regions and the channel region in the course of annealing steps. And the secondary defects due to the ion implantation damage, which may be related to the above-mentioned third drawback, are also generated. In fact, the complex of the secondary defect and the misfit dislocation may be generated. FIG. 7 shows crystal defects of the prior art heterojunction MOSFET with the Si.sub.x Ge.sub.1-x region. The crystal defect region D was generated so as to traverse the pn junction interface 215 over the drain region 206 and the channel region 203. If a (100) plane oriented substrate is used, as shown in FIG. 7, the crystal defects tend to be generated mainly along the [111] planes. In addition, it is hard to control the position and the direction of

crystal defects since they are spread over a wide range. In this case, junction leakage current is increased significantly, and thus the device utility is narrowed. As a result, increase of generation/recombination current, i.e., junction leakage current, with increase of the composition (1-x) of Ge causes a fourth drawback that, in memory device such as DRAM, degradation in data holding characteristic of the cell is caused or manufacturing yield is lowered seriously. It may be true that the defects of this fourth drawback can be overcome by placing the SiGe layer in the source region completely. However, in order to suppress effectively the floating body effect in the SOI.MOSFET, the SiGe layer must be formed sufficiently close to the pn junction interface formed between the source region and the channel region as understood from the potential profile (band diagram) in FIG. 4B. And if we employ the configuration that the SiGe layer is close to the pn junction interface, in some cases, the crystal defects enter into the channel region to generate the high leakage current. It has been experimentally found by inventors of the present invention that, especially under the condition that Ge mole fraction is higher than 20.about.30% or more, dislocations are brought about in the SOI film owing to film distortion, thus preventing attainment of narrow bandgap semiconductor region, which prevents the elimination of the following body effect.